

3530 U.S. PTO

09/363277

07/28/99

FIG 1

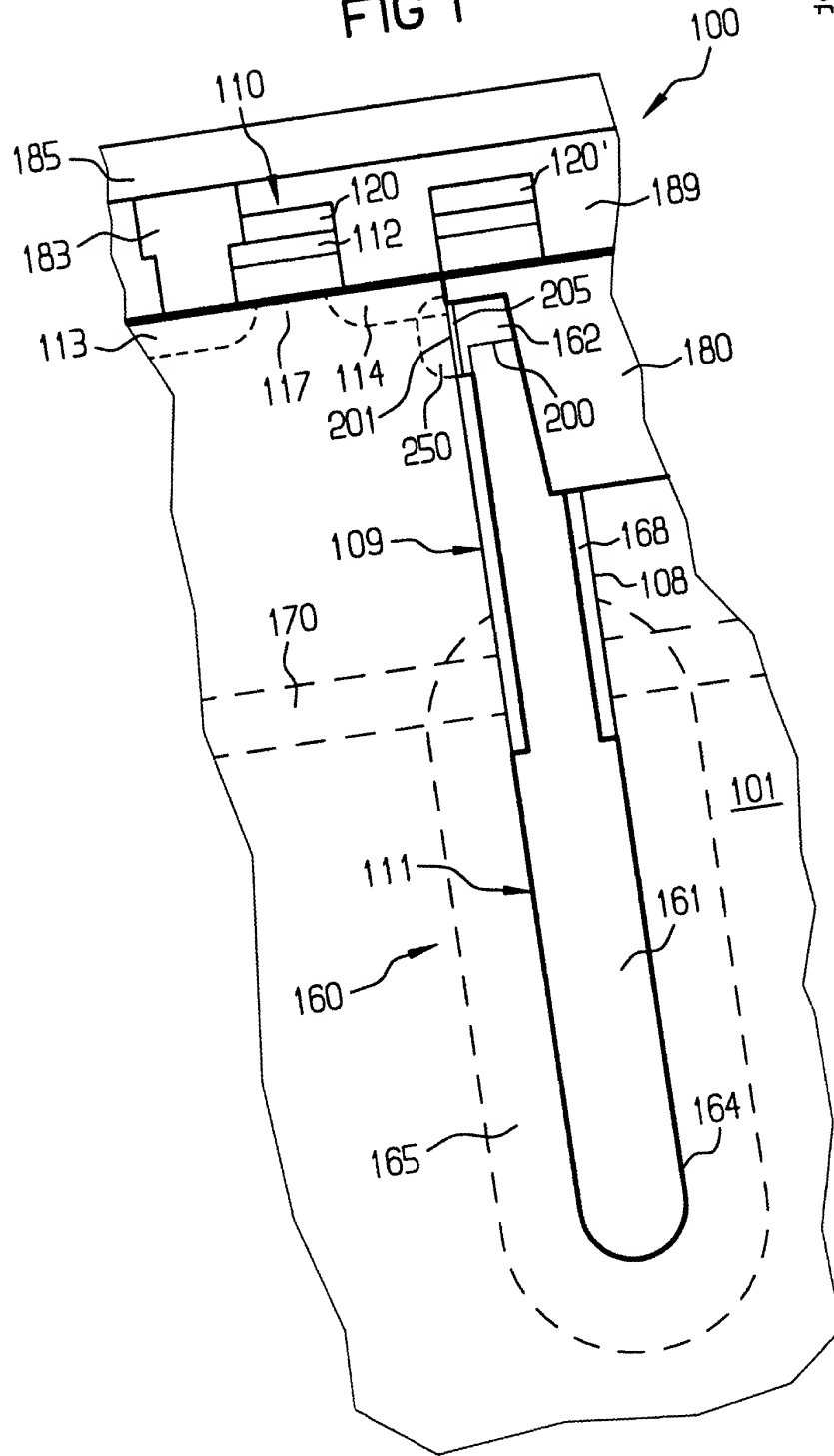


FIG 2a

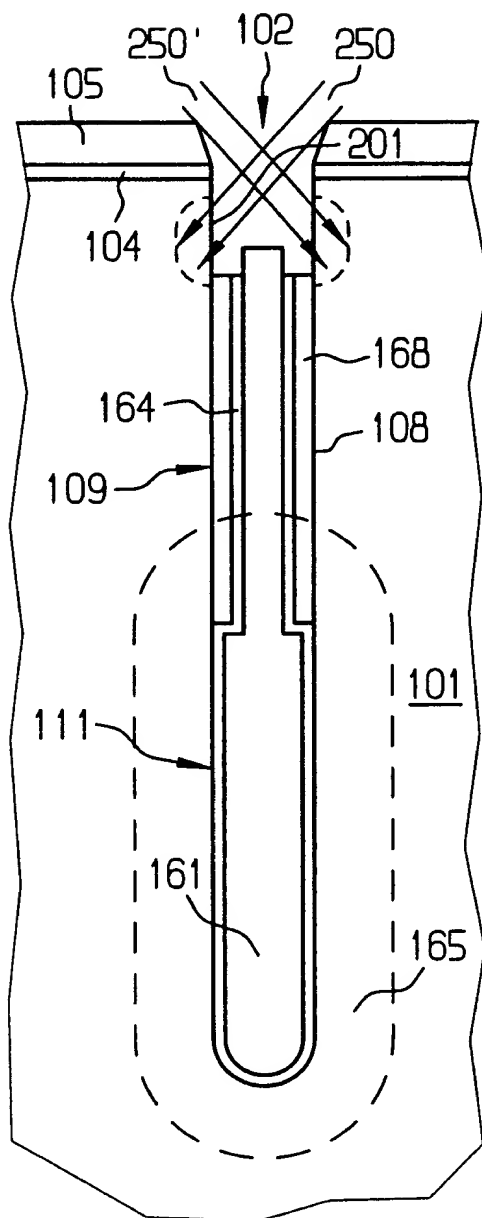


FIG 2b

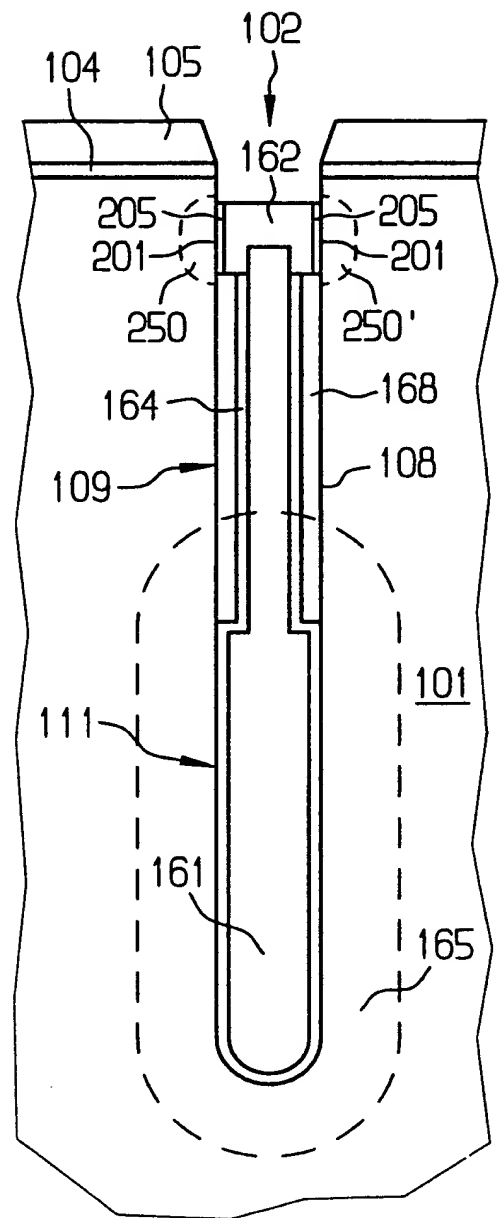
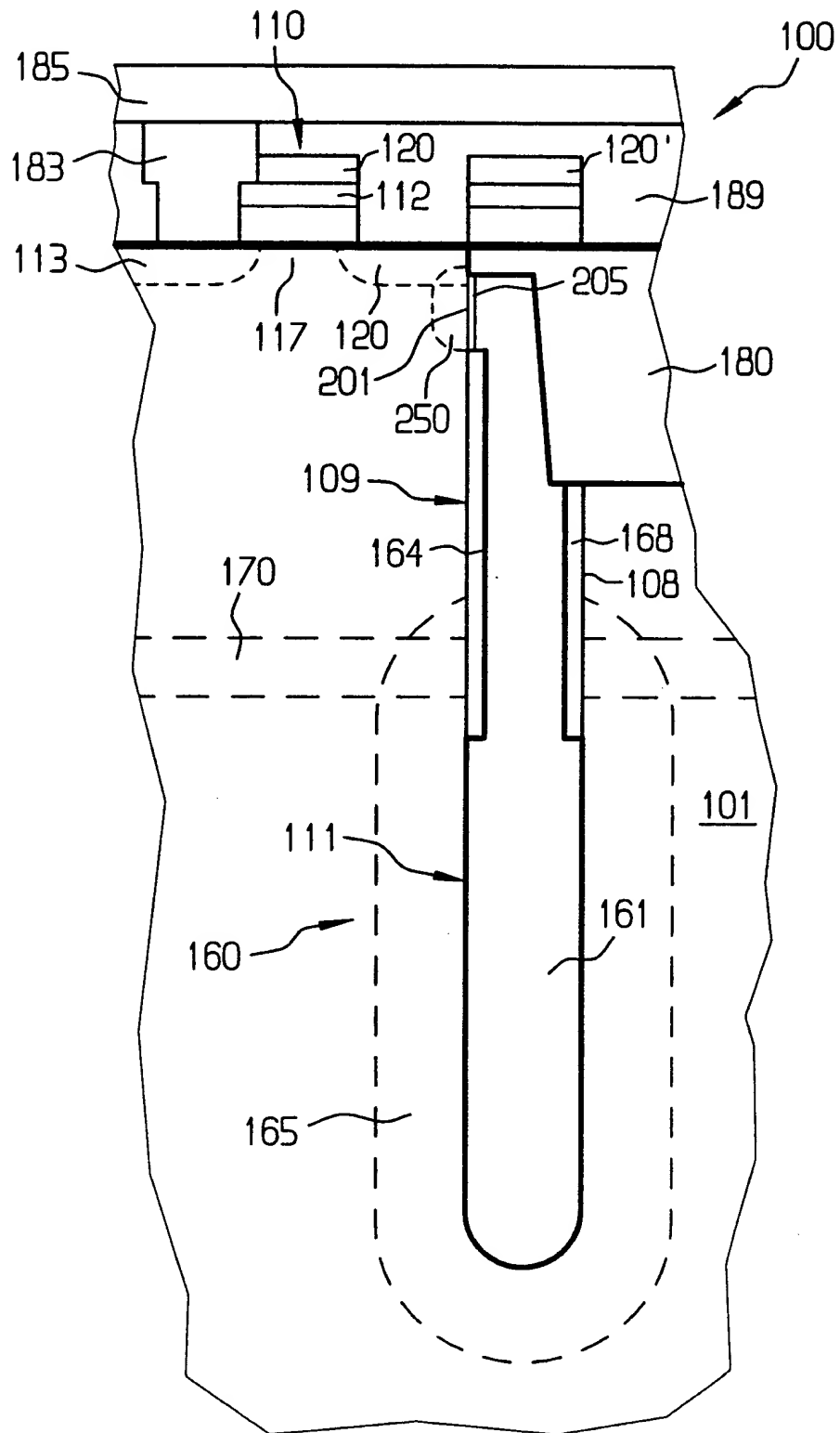


FIG 3



A cross-sectional view of a semiconductor device. A central trench (102) is formed in a substrate (101). The trench is lined with a material (108) and has a bottom layer (161). The side walls of the trench are labeled 164 and 168. The top of the trench is covered by a layer (109). The top surface of the device is labeled 104 and 105. The bottom of the trench is labeled 165. The side walls are also labeled 201 and 205. The bottom of the trench is labeled 111.

FIG 5

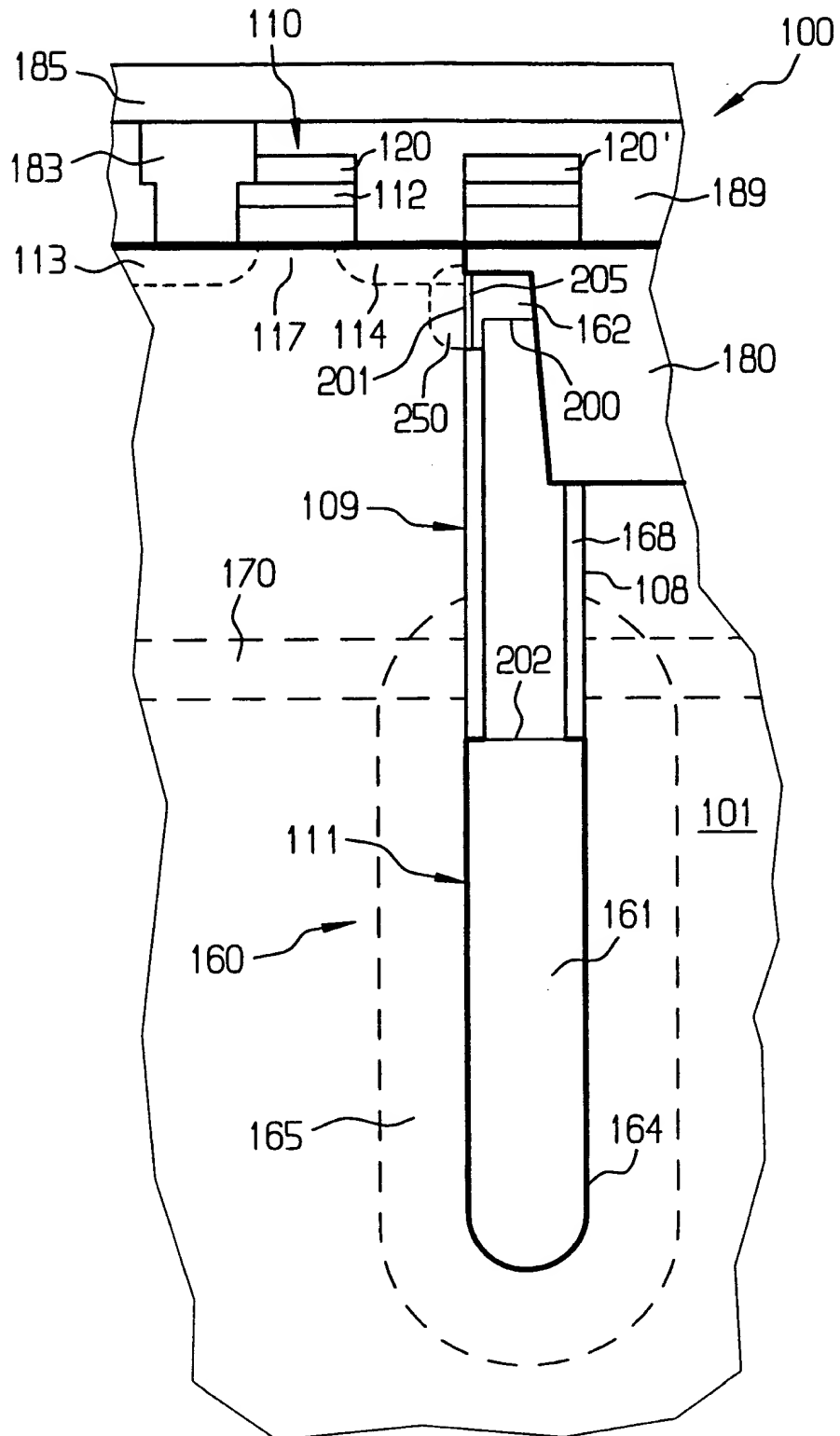


FIG 6

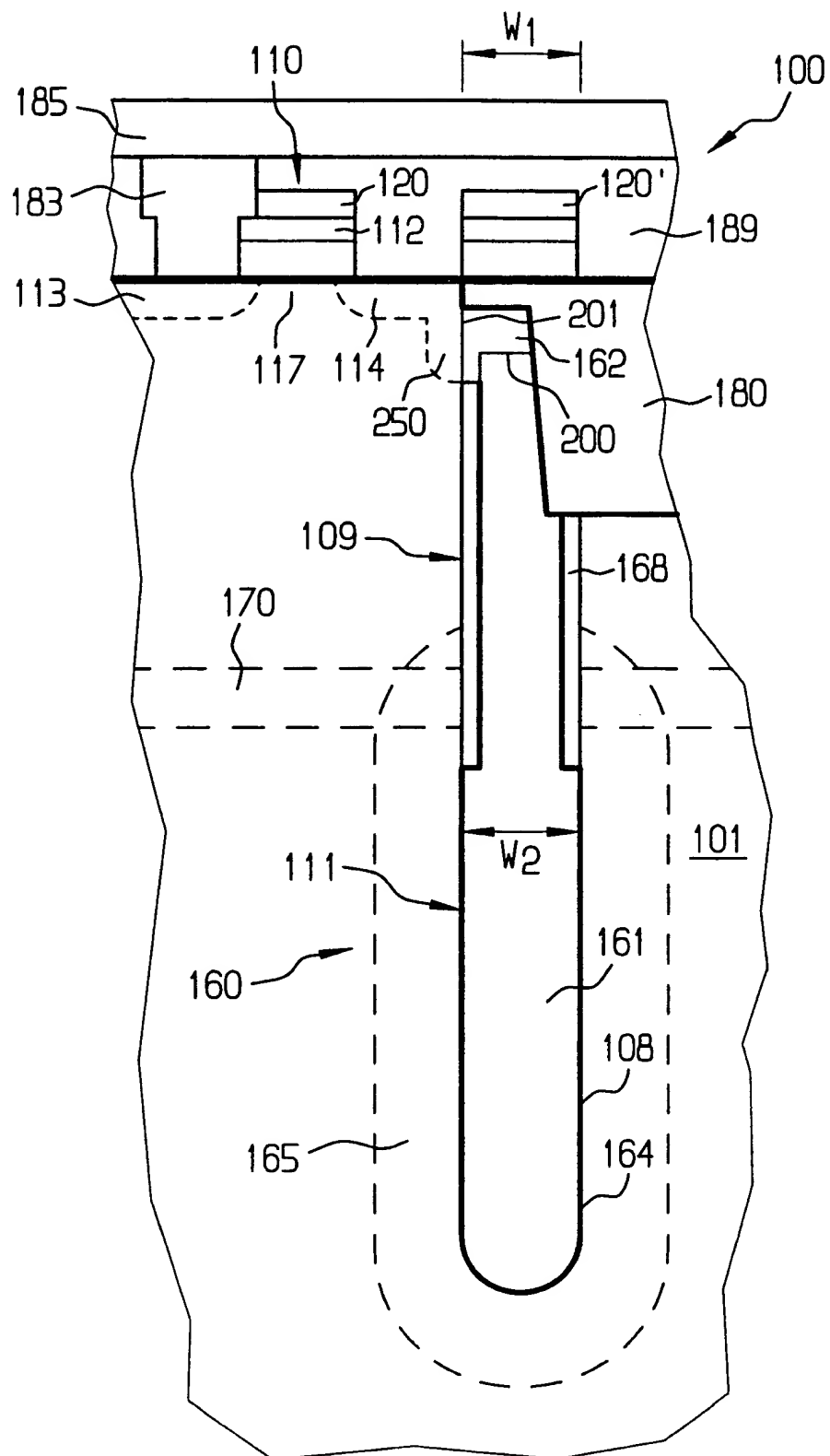


FIG 7 a

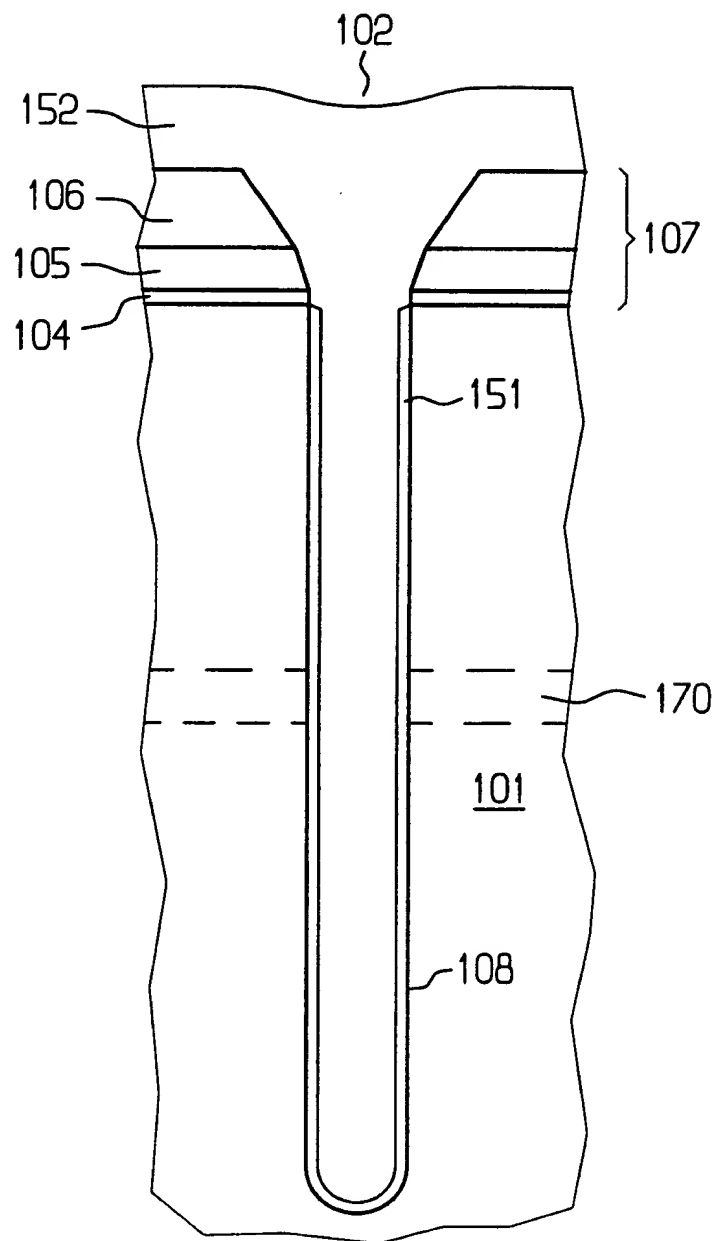


FIG 7 b

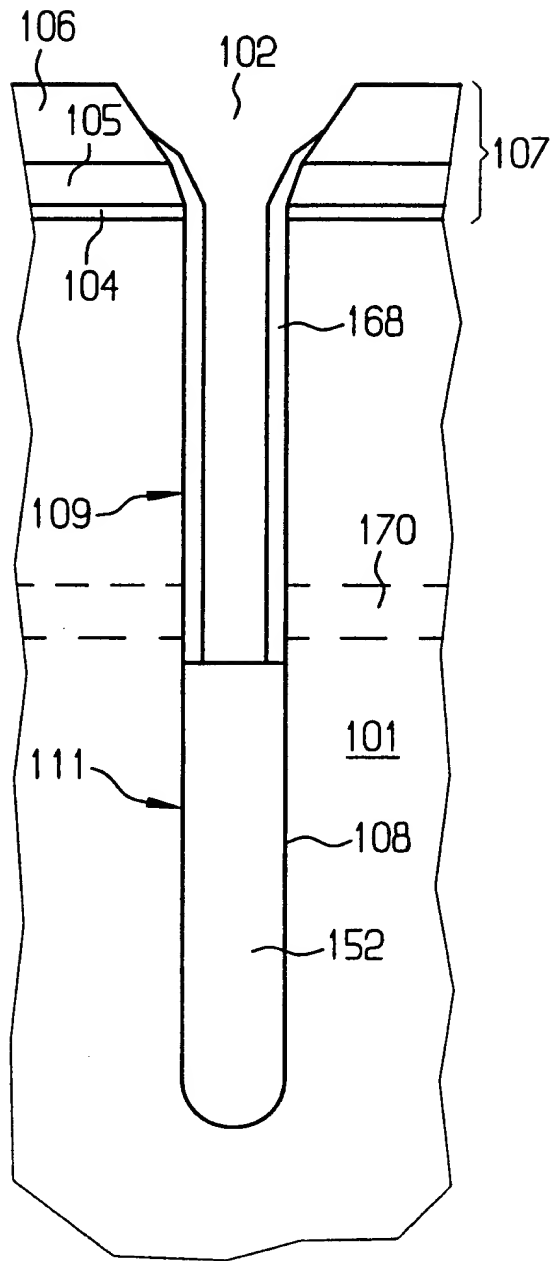


FIG 7 c

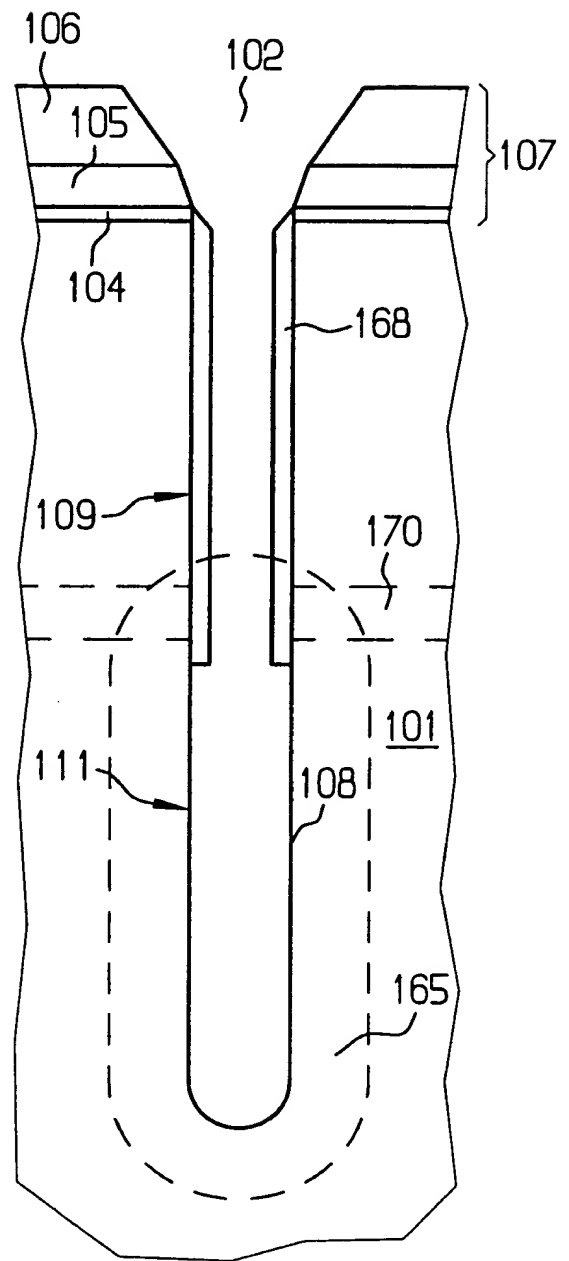




FIG 7d

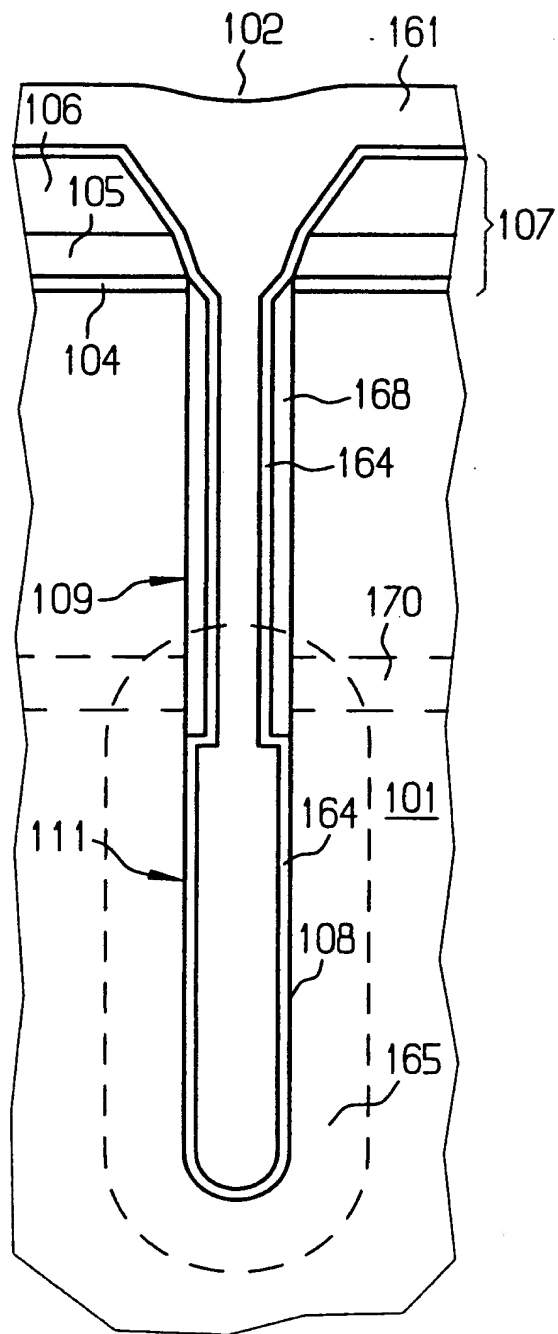


FIG 7e

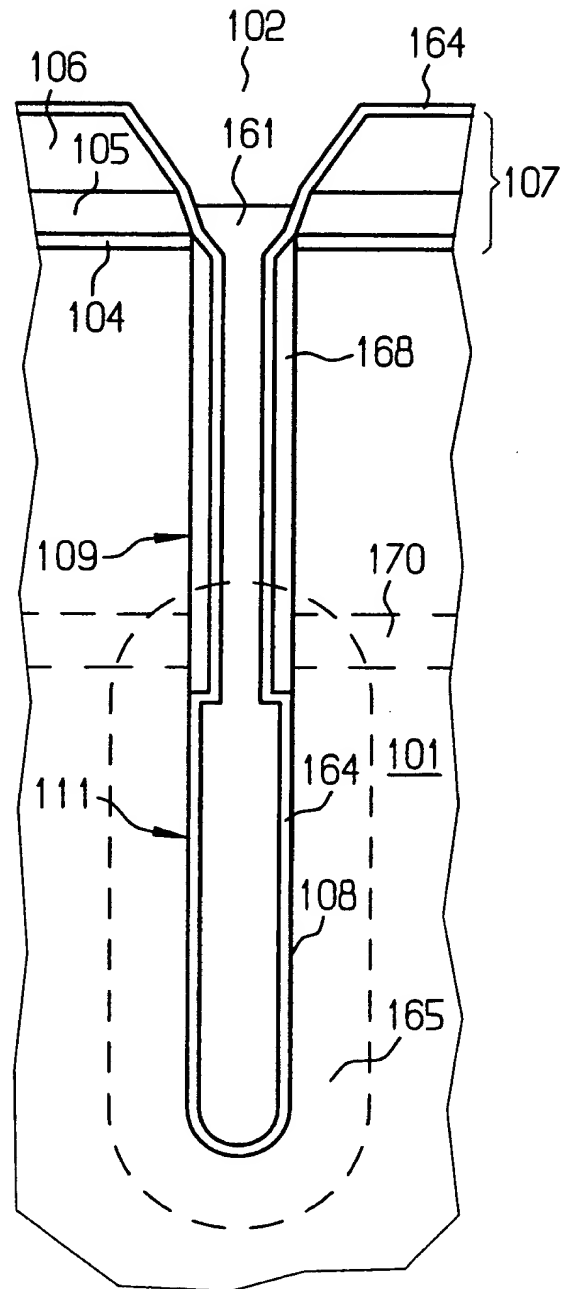


FIG 7f

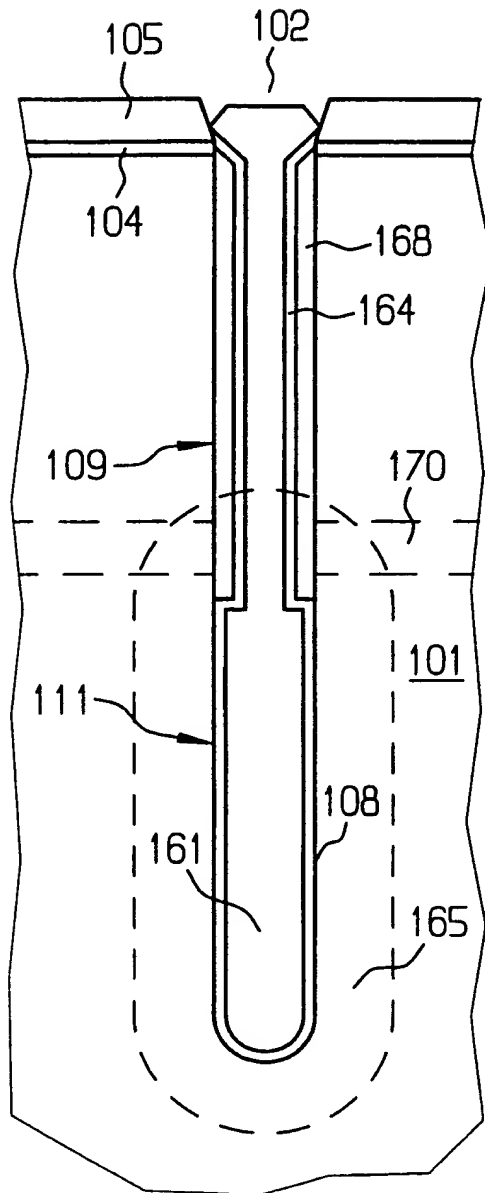


FIG 7g

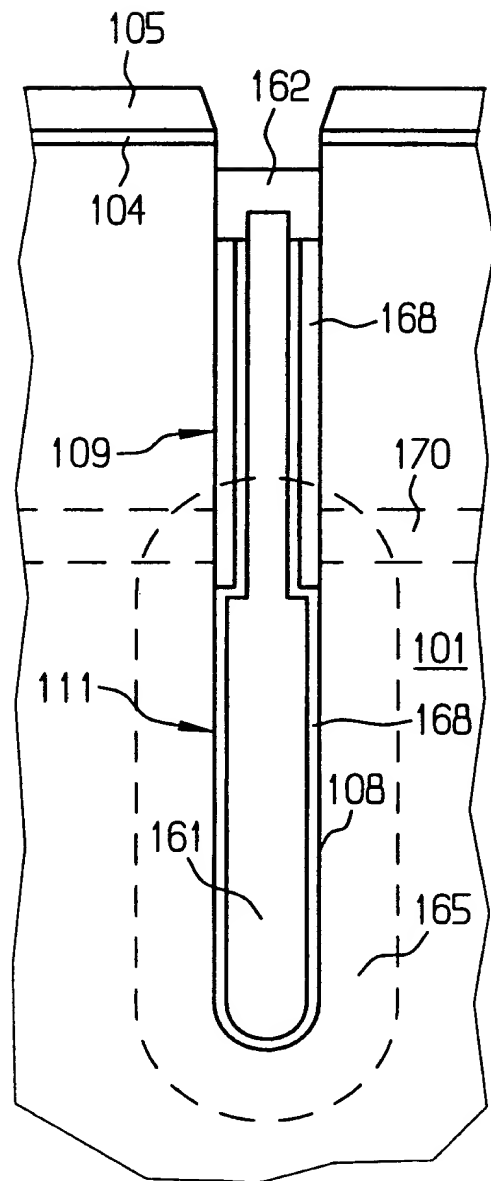


FIG 8

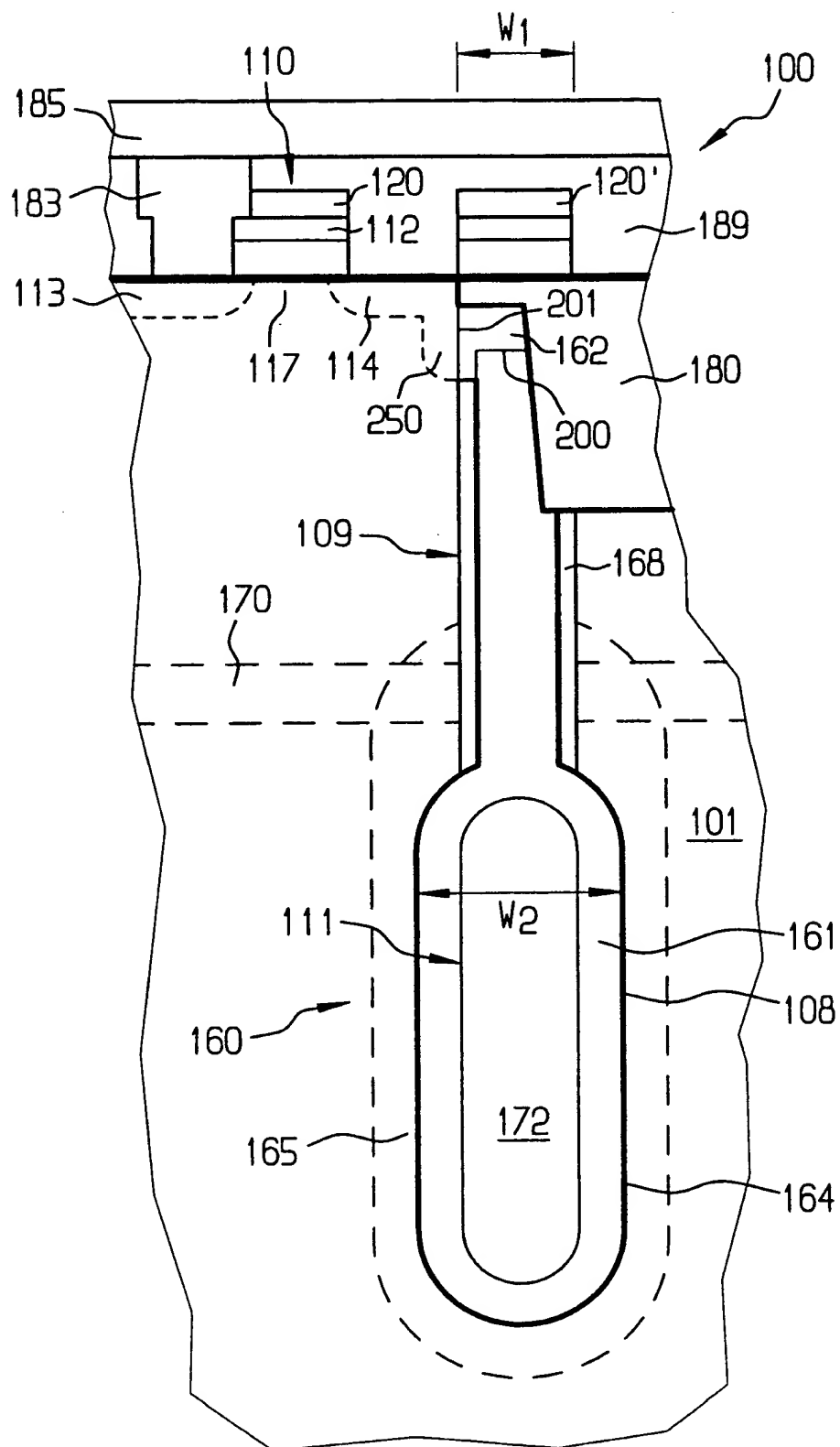


FIG 9

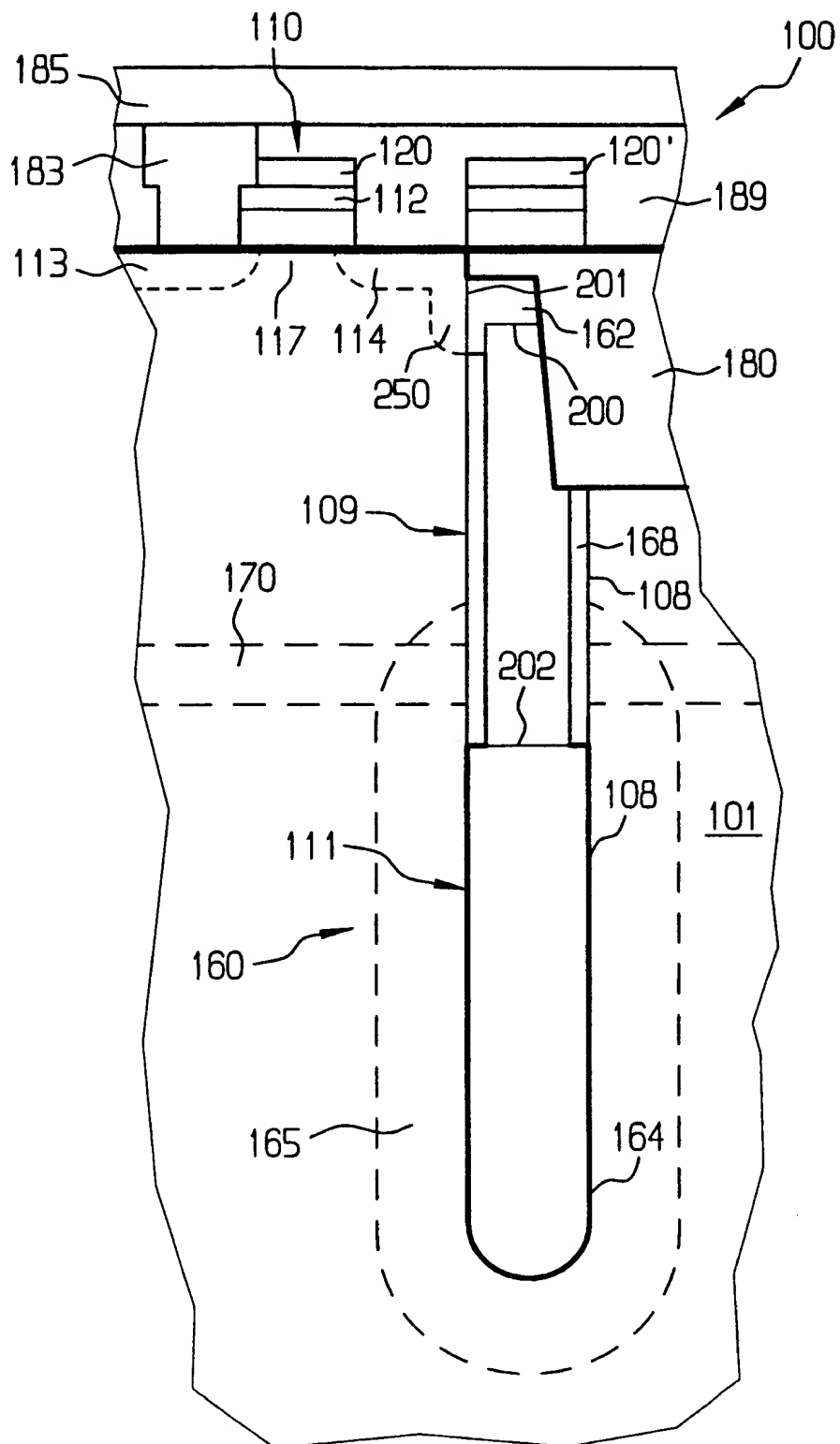


FIG 10

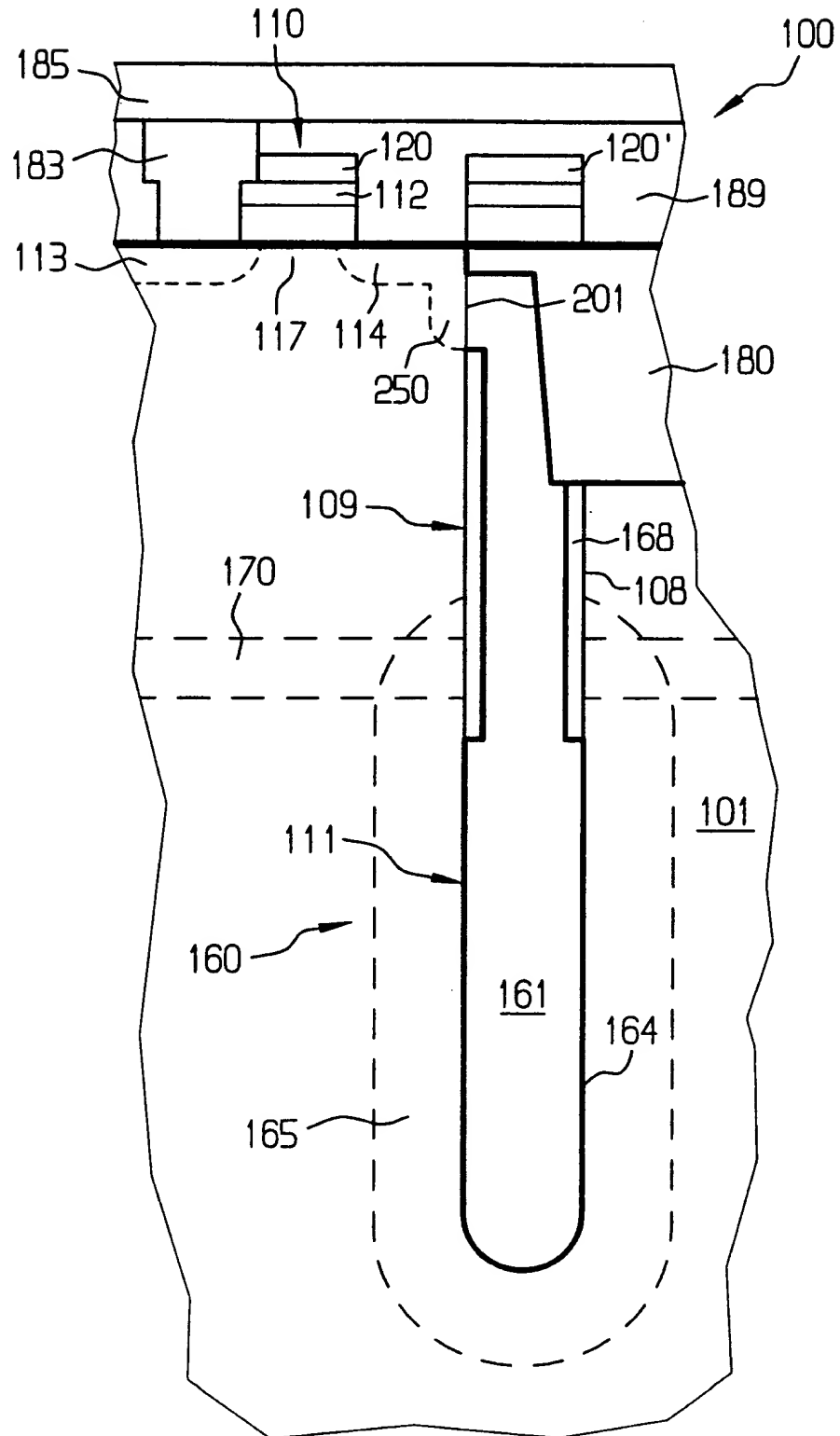


FIG 11a

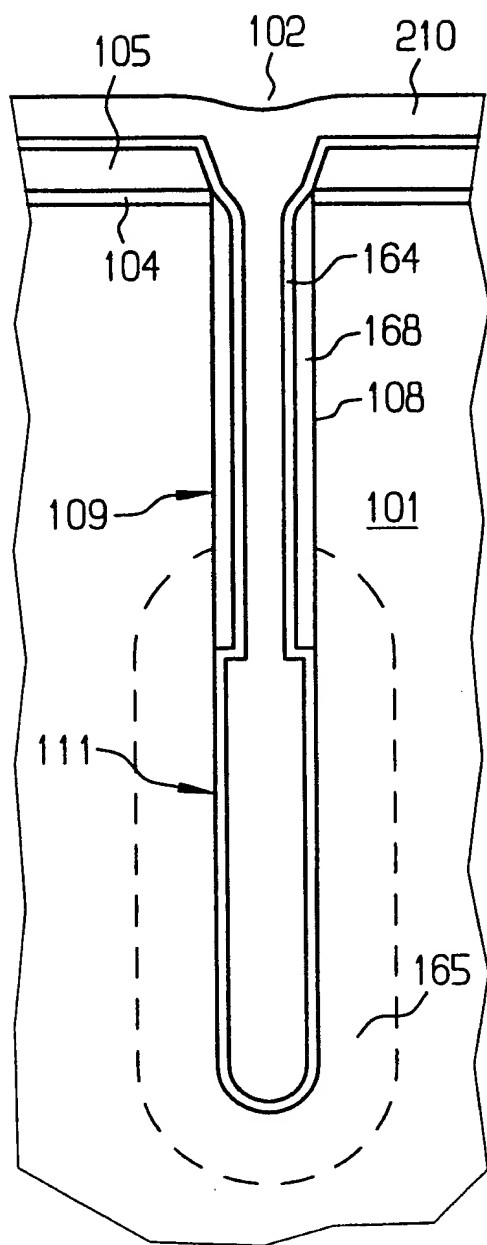


FIG 11b

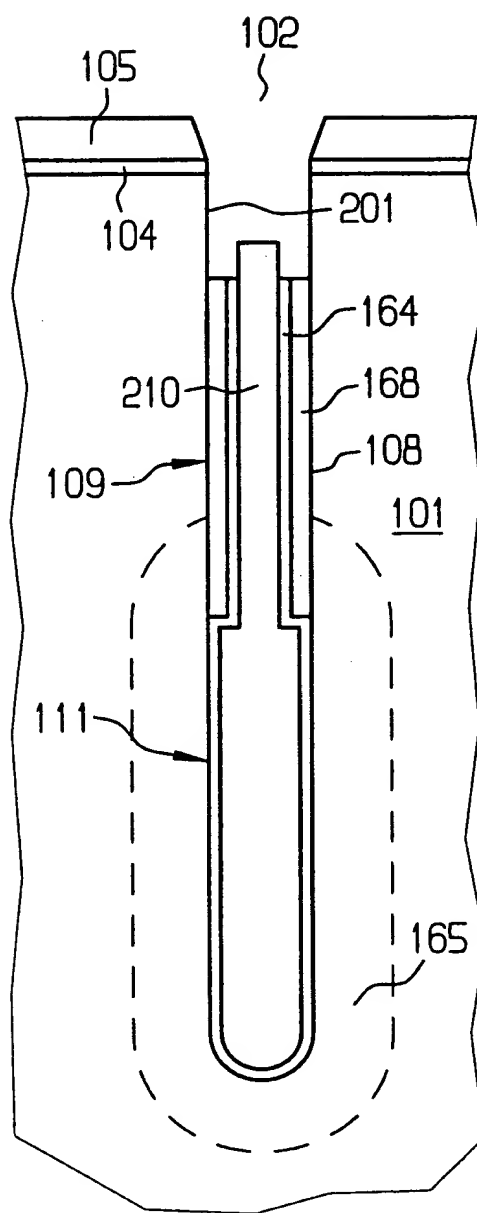


FIG 11c

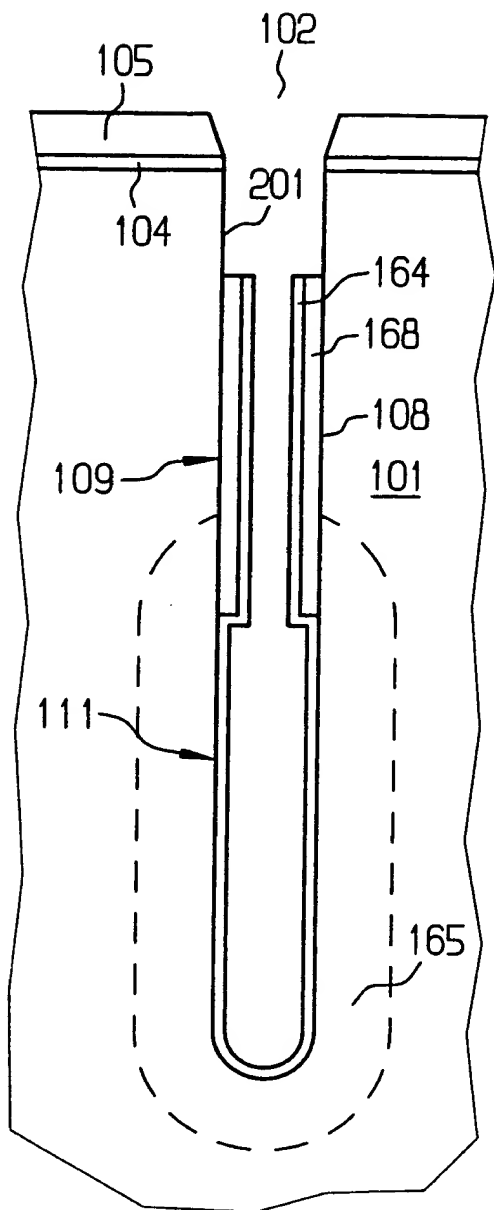


FIG 11d

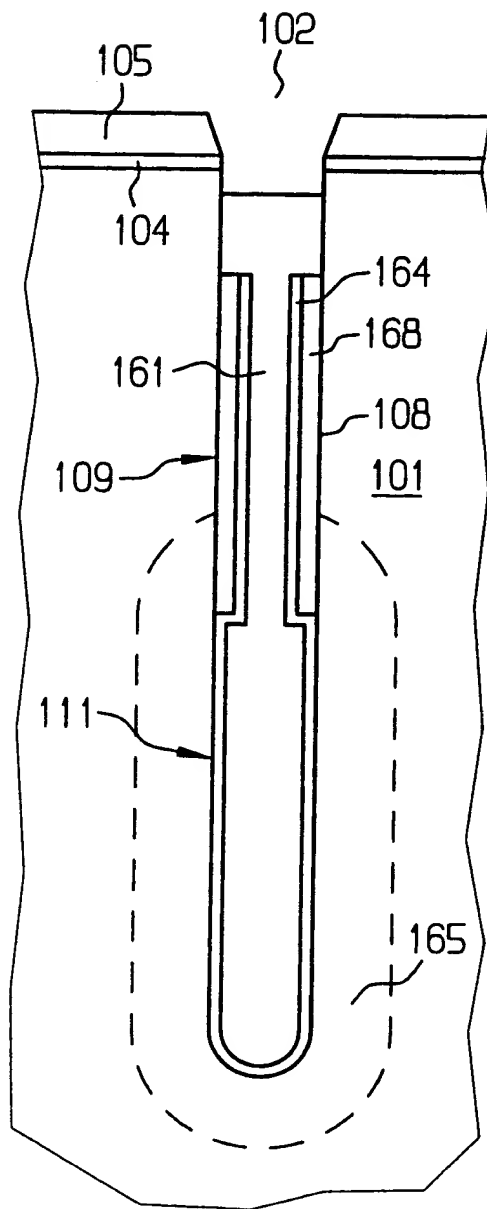


FIG 12

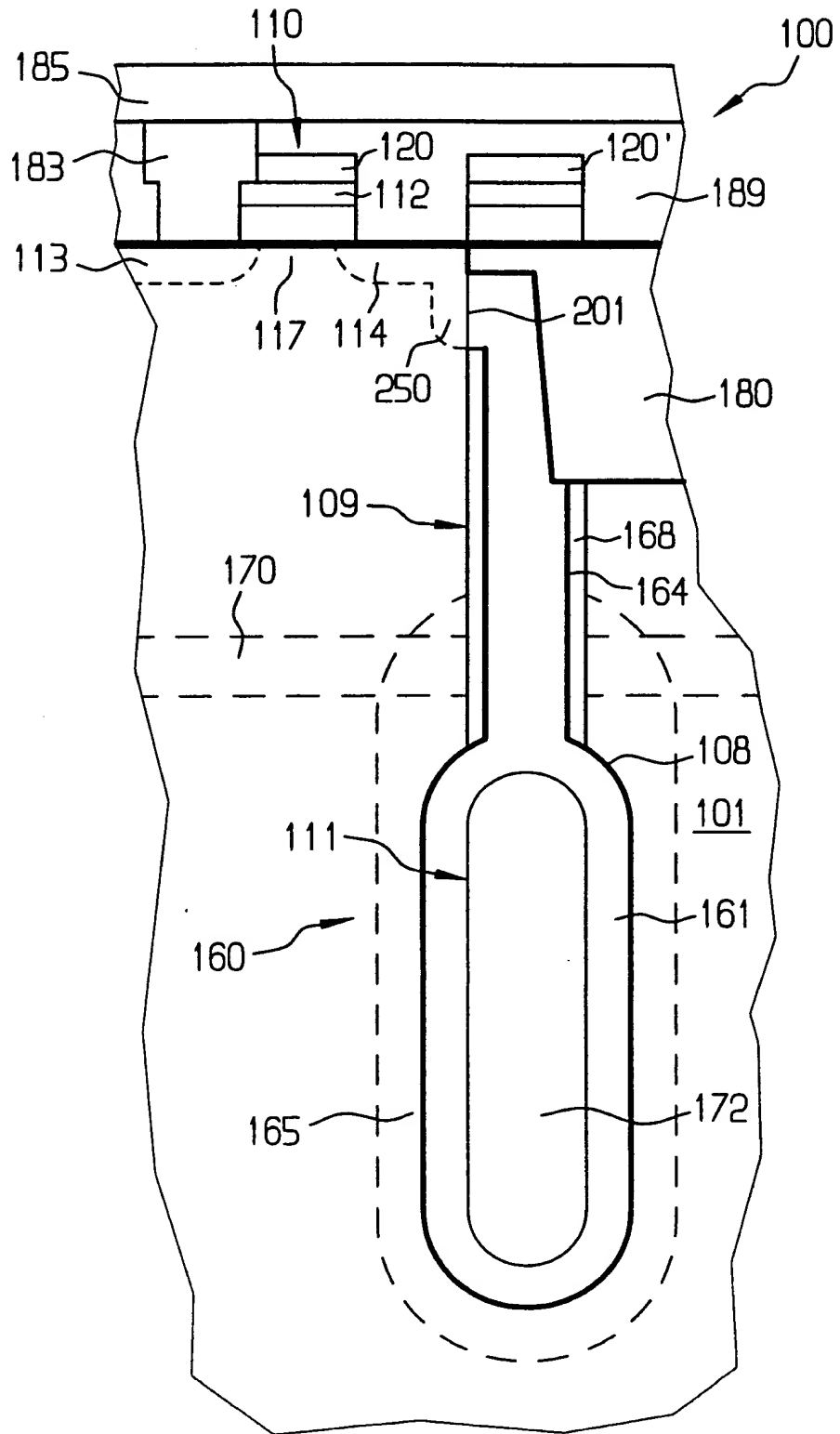




FIG 13

